## HRITVIK TANEJA

Education	<b>Georgia Institute of Technology</b> , Atlanta, GA Ph.D. in Computer Science, 2022 - 2027 (Expected)	
	Indian Institute of Technology Kanpur, India B.Tech. in Computer Science and Engineering, 2016-2020, CGPA: 8.8/10	
Publications	1. Hritvik Taneja, Moinuddin Qureshi "DREAM: Enabling Low-Overhead Rowham- mer Mitigation via Directed Refresh Management" <i>ISCA</i> , 2025	
	2. Hritvik Taneja, Moinuddin Qureshi "RogueRFM: Attacking Refresh Management for Covert-Channel and Denial-of-Service" <i>under Submission</i>	
	3. <b>Hritvik Taneja</b> , Ali Hajiabadi, Michele Marazzi, Kaveh Razavi, Moinuddin Qureshi "All You Need is ALERT: Enabling Space-Time Efficient In-DRAM Mitigation" un- der Submission	
	4. <b>Hritvik Taneja</b> , Jason Kim, Jie Jeff Xu, Stephan van Schaik, Daniel Genkin, Yuval Yarom "Hot Pixels: Frequency, Power, and Temperature Attacks on GPUs and Arm SoCs" USENIX Security, 2023	
	5. Arpit Gupta, Parv Mor, <b>Hritvik Taneja</b> , Biswabandan Panda "STEVES: Pushing the Limits of Value Predictors with Sliding FCM and EVES" <i>Championship Value</i> <i>Prediction</i> , 2019	
Research Experience	<b>Graduate Research Assistant</b> Georgia Institute of Technology Advisor: Professor Moinuddin Qureshi Research Focus: Memory system optimizations for M	December 2023 - Present Atlanta, GA L workloads
	<b>Graduate Research Assistant</b> Georgia Institute of Technology Advisor: Professor Daniel Genkin Research Focus: Side-channel attacks	August 2022 - November 2023 Atlanta, GA
Professional Experience	<ul> <li>Advanced Design Verification Intern</li> <li>Astera Labs</li> <li>□ Developed a tool for large-scale Verilog simulation</li> <li>□ Focused on improving the cost efficiency by reductivity lizing spot instances.</li> </ul>	May 2024 - Aug 2024 Santa Clara, CA s on an AWS-backed cluster. ing the unused memory and uti-
	Infrastructure Developer       Jan 2020 - Dec 2021         Plutus Research Private Limited       Bengaluru, India         □ Improved latency of market-data arrival to high-frequency trading (HFT) strategies         — by 20% in median and by 30% in 90 percentile.         □ Developed an approximate backtesting framework that uses snapshots of the price-level order book to generate trade responses — with minimal deviation in the fill ratio.	
	<ul> <li>Software Engineering Intern</li> <li>Nutanix, Inc.</li> <li>Improved the average turnaround time of the Nucaching responses.</li> <li>Use gossip protocol to ensure cache consistency, in</li> <li>Worked on bug fixes and implemented new feature part of the Nutanix CALM team.</li> </ul>	May 2019 - Jul 2019 Bengaluru, India utanix Calm API by 80 fold, by a scaled-out setup. ures in frontend and backend, as

**Backend Developer** May 2017 - July 2017 New York Office, IIT Kanpur Kanpur, India □ Worked on a scalable microservice based web application with an extensive technology stack. □ Used Scala with Akka, Facebook's Phabricator among other technologies for developing the backend. Hardware Security Lab August 2022 - February 2023 Georgia Institute of Technology Atlanta, GA □ Discovered and evaluated the data-dependent nature of frequency scaling on GPUs and Arm SoCs. □ Exploited this phenomenon to mount Pixel Stealing, History Sniffing, and Website Fingerprinting attacks on various devices. □ Apple assigned us CVE-2023-38599 for our work. **Championship Value Prediction** Dec 2018 - Jun 2019 Indian Institute of Technology Kanpur Kanpur, India □ Proposed and built an FCM based value predictor, which achieves an improvement of 1.4% over state-of-the-art EVES predictor. □ Secured first (currently third) position on the unlimited track leaderboard of CVP from May'19 to November'19. **NINE LLCs in Multicore Processors** Aug 2019 - Nov 2019 Indian Institute of Technology Kanpur Kanpur, India □ Designed a non-inclusive non-exclusive LLC, which marks each block either as inclusive or exclusive in a multi-core processor. □ Implemented a cache simulator equipped with MESI cache coherence protocol to analyze performance counters like messages & misses. □ Improved the performance in terms of private cache misses, LLC misses, and number of interconnect messages – **Report**. **Inter-Procedural Data-flow Analysis** Aug 2019 - Nov 2019 Indian Institute of Technology Kanpur Kanpur, India □ Ported and implemented the inter-procedural analysis from [PadhyeK13] to LLVM (originally in Soot). □ Modified the framework [PadhyeK13] to account for fundamental differences between Soot and LLVM □ Designed and implemented a sign data-flow analysis using the same framework – Code. **Golang Compiler** Jan 2019 - April 2019 Indian Institute of Technology Kanpur Kanpur, India  $\Box$  A compiler for go written in go as a course project for compilers. Compiles from golang to x86 assembly. □ Supports a subset of the go language, including pointers, type checking, recursion, and some other common language features – Code. **Proficient:** C/C++, Python, Pytorch

Key

Projects

Skills